AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a sampler circuit configured to generate a digital signal in response to a pre-amplified signal; and

a filter circuit configured to generate a track ID signal in response to said digital signal, wherein said filter circuit is configured ~~to~~ (i) as a three-tap filter ~~improve or increase signal-to-noise ratio (SNR)~~ and (ii) to reject a DC offset ~~errors~~ error in said digital signal.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said filter circuit is further configured to implement ~~simple~~ each tap multiplication coefficients as an integer.

3. (ORIGINAL) The apparatus according to claim 1, wherein said filter circuit is configured to implement multiplication coefficients of one.

4. (ORIGINAL) The apparatus according to claim 1, wherein said filter circuit is immune to DC offsets and shifts from thermal asperities.

5. (ORIGINAL) The apparatus according to claim 1, wherein said filter circuit is further configured to attenuate high frequencies.

6. (ORIGINAL) The apparatus according to claim 5, wherein said filter circuit is configured to reject low frequencies.

7. (ORIGINAL) The apparatus according to claim 1, wherein said filter circuit is further configured to closely match said digital signal.

8. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said sampler circuit comprises:

a voltage gain amplifier configured to receive said pre-amplified signal; and

a magneto-resistive head asymmetry correction circuit coupled to said voltage gain amplifier~~;~~

~~a continuous time filter coupled to said magnetic-resistive asymmetry correction circuit;~~

~~an offset cancellation circuit coupled to said continuous time filter; and~~

~~an analog to digital conversion circuit configured to generate said digital signal and coupled to said offset cancellation circuit~~.

9. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said filter circuit comprises:

a digital filter circuit configured to generate a filtered track ID signal; and

~~a track ID decoder configured to generate said track ID signal in response to said filtered track ID signal;~~

a position error signal (PES) filter configured to generate a filtered PES signal in response to said digital signal~~;~~ ~~and~~

~~a PES demodulator configured to generate a PES signal in response to said filtered PES signal~~.

10. (ORIGINAL) The apparatus according to claim 1, further comprising:

a read channel circuit configured to generate a read data signal in response to said digital signal.

11. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said filter circuit comprises:

~~one or more~~ a plurality of delay elements configured to delay said digital signal; and

a summation circuit configured to perform summation of said delayed digital signals and provide an output filtered signal.

12. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said filter circuit comprises:

a first delay element configured to receive said digital signal and present a first delayed signal;

a second delay element configured to receive said first delayed signal and present a second delayed signal; and

a shift left circuit configured to receive said second delayed signal and present a shifted signal~~; and~~

~~a summation circuit configured to receive said digital signal, said first delayed signal and said shifted signal and generate a filtered output signal~~.

13. (CURRENTLY AMENDED) The apparatus according to claim ~~12~~ 1, wherein said filter circuit comprises a first and a second ~~delay elements comprise~~ 4th order delay elements.

14. (ORIGINAL) The apparatus according to claim 1, wherein said track ID signal comprises a servo track ID signal.

15. (ORIGINAL) The apparatus according to claim 1, wherein said filter circuit comprises:

a servo track ID filter configured to generate said track ID signal in response to said digital signal.

16. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a digital signal in response to a pre-amplified signal;

means for generating a track ID signal in response to three-tap filtering said digital signal;

~~means for providing improved signal-to-noise ratio (SNR);~~ and

means for rejecting a DC offset error in said digital signal.

17. (CURRENTLY AMENDED) A method for improved filter bi-phase servo demodulation, comprising the steps of:

(A) generating a digital signal in response to a pre-amplified signal;

(B) generating a track ID signal in response to three-tap filtering said digital signal ~~filtering a digital signal~~; and

(C) ~~providing improved signal-to-noise ratio (SNR) and~~ rejecting a DC offset error in said digital signal.

18. (CURRENTLY AMENDED) The method according to claim 17, wherein ~~step (C) further comprises:~~

~~implementing simple~~ all tap multiplication coefficients of said three-tap filtering comprise integers.

19. (CURRENTLY AMENDED) The method according to claim 17, wherein step ~~(C)~~ (B) further comprises the sub-steps of:

delaying said digital signal to generate a first delayed signal;

delaying said first delayed signal to generate a second delayed signal; and

shifting said second delayed signal to generate a shifted signal~~; and~~

~~summing said digital signal, said first delayed signal and said shifted signal to generate a filtered output signal~~.

20. (ORIGINAL) The method according to claim 17, wherein step (C) further comprises:

attenuating high frequencies; and

rejecting low frequencies.

21. (NEW) The apparatus according to claim 1, wherein said filter circuit is configured as a 1+D-2D^2 filter.

22. (NEW) The apparatus according to claim 1, wherein said track ID signal has a signal-to-noise ratio of at least 23.58 dB.

23. (NEW) The apparatus according to claim 8, wherein said sampler circuit further comprises:

a continuous time filter coupled to said magnetic-resistive asymmetry correction circuit;

an offset cancellation circuit coupled to said continuous time filter; and

an analog to digital conversion circuit configured to generate said digital signal and coupled to said offset cancellation circuit.

24. (NEW) The apparatus according to claim 9, wherein said filter circuit further comprises:

a track ID decoder configured to generate said track ID signal in response to said filtered track ID signal; and

a PES demodulator configured to generate a PES signal in response to said filtered PES signal.

25. (NEW) The apparatus according to claim 12, wherein said filter circuit further comprises:

a summation circuit configured to generate a filtered output signal by summing said digital signal, said first delayed signal and said shifted signal.

26. (NEW) The method according to claim 19, wherein step (B) further comprises the sub-step of:

summing said digital signal, said first delayed signal and said shifted signal to generate a filtered output signal.

27. (NEW) the method according to claim 17, wherein said three-tap filtering comprises a $1+D^4-2D^8$ filtering.